PTO/SB/50 (06-03)
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REISSUE PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	MTKR001
First Named Inventor	CHEN, Joe
Original Patent Number	6,507,881
Original Patent Issue Date (Month/Day/Year)	Jan. 14, 2003
Express Mail Label No.	ER 208807615 US

APPLICATION FOR REISSUE OF: *(Check applicable box)* ☑ Utility Patent ☐ Design Patent ☐ Plant Patent

APPLICATION ELEMENTS (37 CFR 1.173)

1. ☑ Fee Transmittal Form *(PTO/SB/56)* *(Submit an original, and a duplicate for fee processing)*
2. ☐ Applicant claims small entity status. See 37 CFR 1.27.
3. ☑ Specification and Claims in double column copy of patent format *(amended, if appropriate)*
4. ☑ Drawing(s) *(proposed amendments, if appropriate)*
5. ☑ Reissue Oath/Declaration (original or copy) (37 CFR 1.175) *(PTO/SB/51 or 52)*
6. ☑ Power of Attorney
7. ☑ Original U.S. Patent currently assigned? ☑ Yes ☐ No *(If Yes, check applicable box(es))*
   - ☑ Written Consent of all Assignees *(PTO/SB/53)*
   - ☑ 37 CFR 3.73(b) Statement (PTO/SB/96)
8. ☐ CD-ROM or CD-R in duplicate, Computer Program (Appendix) or large table
9. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all of the following are necessary)*
   - a. ☐ Computer Readable Form (CFR)
   - b. Specification Sequence Listing on:
     - i ☐ CD-ROM (2 copies) or CD-R (2 copies); or
     - ii ☐ paper
   - c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

10. ☑ Statement of status and support for all changes to the claims. See 37 CFR 1.173(c).
11. ☐ Original Patent Grant
    - ☐ Ribboned Original Patent Grant
    - ☐ Statement of Loss (PTO/SB/55)
12. ☐ Foreign Priority Claim *(35 U.S.C. 119)* *(if applicable)*
13. ☑ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
14. ☐ English Translation of Reissue Oath/Declaration *(if applicable)*
15. ☐ Preliminary Amendment
16. ☑ Return Receipt Postcard *(MPEP 503)* *(Should be specifically itemized)*
17. Other: _____

18. CORRESPONDENCE ADDRESS

☑ *Customer Number:* 33392 **OR** ☐ *Correspondence address below*

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Elizabeth Chien-Hale	*Registration No.* (Attorney/Agent)	44,077
Signature	Elizabeth Chien-Hale	*Date*	March 20, 2004

This collection of information is required by 37 CFR 1.173. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Reissue, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/56 (08-03)
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REISSUE APPLICATION FEE TRANSMITTAL FORM

Docket Number (Optional): MTKR001

Claims as Filed – Part 1

	(1) Claims in Patent	(2) Number Filed in Reissue Application	(3) Number Extra	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	(A) 18	(B) 40	**** 22 =	x $ ___ =			x $ 18 =	396
Independent claims (37 CFR 1.16(i))	(C) 2	(D) 4	* 2 =	x $ ___ =		or	x $ 86 =	172
			Basic Fee (37 CFR 1.16(h))		$ ____			$ 770
			Total Filing Fee		$ ____		OR	$ 1338

Claims as Amended – Part 2

	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Extra Claims Present	Small Entity Rate	Small Entity Fee		Other than a Small Entity Rate	Other than a Small Entity Fee
Total Claims (37 CFR 1.16(j))	***	MINUS	**	* =	X $ ____ =			x $ ____ =	
Independent Claims (37 CFR 1.16(i))	***	MINUS	*****	=	x $ ____ =			x $ ____ =	
				Total Additional Fee		$		OR	$

* If the entry in (D) is less than the entry in (C), Write "0" in column 3.

** If the "Highest Number of Total Claims Previously Paid For" is less than 20, Write "20" in this space.

*** After any cancellation of claims.

**** If "A" is greater than 20, use (B – A); if "A" is 20 or less, use (B – 20).

***** "Highest Number of Independent Claims Previously Paid For" or Number of Independent Claims in Patent (C).

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ Please charge Deposit Account Number _____ in the amount of _____.
A duplicate copy of this sheet is enclosed.

☐ The Director is hereby authorized to charge any additional fees under 37 CFR 1.16 or 1.17 which may be required, or credit any overpayment to Deposit Account Number _____.
A duplicate copy of this sheet is enclosed.

☒ A check in the amount of $ 1,338.00 to cover the filing/additional fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

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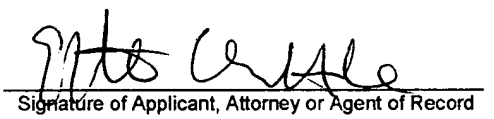
March 20, 2004
Date


Signature of Applicant, Attorney or Agent of Record

44,077
Registration Number, if applicable

Elizabeth Chien-Hale
Typed or printed name

PATENT
Docket No. MTKR001
Reissue Application
Docket No.: MTKR001

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Express Mail Label No.: ER 208807615 US Date of Deposit: March 20, 2004

I Elizabeth Chien-Hale hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on March 20, 2004.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Joe Chen

Patent No.: 6,507,881

Issue Date: January 14, 2003

Reissue App. No.: Not Yet Assigned

Filing Date: Herewith

For: METHOD AND SYSTEM FOR PROGRAMMING A PERIPHERAL FLASH MEMORY VIA AN IDE BUS

Examiner: Not Yet Assigned

Group Art Unit: Not Yet Assigned

STATUS OF CLAIMS AND SUPPORT FOR CLAIMS CHANGES UNDER 37 CFR §1.173(c)

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Alexandria, Virginia 22313-1450

Dear Sir:

The status of the claims as a result of the amendment submitted herewith in:

Claims cancelled: 0

Claims amended: 0

Claims added: 19-40

The support in the disclosure of the patent for the claims added is as follows:

Claim No.	Location is the issued patent
19	Col. 3, lines 63-67, Col. 4, lines 1-17, of the '881 patent
20	Col. 7, lines 23-29
21	Col. 8, lines 23-25
22	Col. 4, lines 21-25
23	Col. 5, lines 43-53
24	Col. 3, lines 62-67
25	Col. 7, TABLE 3
26	Col. 6, lines 47-60
27	Col. 10, lines 30-35
28	Col. 7, lines 51-54
29	FIG. 2 and Col. 2, lines 45-61
30	Col. 3, lines 62-67
31	Col. 6, lines 47-60
32	Col. 9, lines 42-46
33	Col. 4, lines 21-25
34	Col. 4, TABLE 1
35	Col. 5, lines 43-53
36	Col. 5, lines 47-50
37	Col. 5, TABLE 2
38	Col. 7. lines 27-29
39	Col. 10, lines 30-35
40	Col. 4, TABLE 3

Dated: March 20, 2004

Respectfully submitted,

By: _____

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19. A method for updating a firmware of a flash read-only memory (ROM), the method being suitable for a host computer (Host) to update the firmware of the flash ROM through an interface comprising ATA task files and a flash controller coupled to the Host through the interface, the method comprising:

entering a flash ROM programming mode by the Host issuing an interface control command with the ATA task files;

disabling access to the flash ROM from a microprocessor so as to perform programming;

entering update information into the flash ROM directly by the Host through the flash controller;

leaving the flash ROM programming mode and returning to a normal mode.

20. The method of claim 19, wherein entering update information into the flash ROM comprises reading or writing data on the flash ROM through a software cycle or a hardware cycle.

21. The method of claim 20, wherein reading or writing data on the flash ROM further comprises assigning an initial address.

22. The method of claim 20, wherein reading or writing data on the flash ROM through the software cycle comprises directly accessing pins of the flash ROM by the Host.

23. The method of claim 20, wherein in the step of reading or writing data on the flash ROM through the hardware cycle comprises temporarily storing the data into a memory buffer and then transferring the data from the memory buffer to the Host or the flash ROM for reading data and writing data respectively.

24. The method of claim 19, wherein the interface is an IDE interface and registers of the task files are redefined in entering the programming mode from definitions of the IDE interface to definitions for updating the flash ROM.

25. The method of claim 24, wherein the registers of the task files comprise:

a DATA register used as a data port and has a same definition in the task files;

a LENGTH register used as a transfer length to specify a transferring byte count of the data in the hardware cycle;

a CTL register defined as a control mapped to the flash ROM pins of cs#, wr#, and oe#, in which the Host can use the CTL register to control or obtain a status of the pins;

a DBUS register defined as a data bus mapped to the flash ROM pins of data bus, in which the Host can use the DBUS register to control or obtain a status of the pins; an accompanying bit is defined to decide the direction of data bus;

an ABUSLOW register defined as an address bus low mapped to the flash ROM pins of an address bus low byte, in which the Host can use the ABUSLOW register to control or obtain a status of the pins;

an ABUSHIGH register defined as an address bus high mapped to the flash ROM pins of an address bus high byte, in which the Host can use the ABUSHIGH register to control or obtain a status of the pins;

a DRIVE-SELECT register defined as a drive select, in which the Host writes the DRIVE_SELECT register to select an IDE periphery device, and DRIVE_SELECT register has a same definition in the task files; and

a COMMAND/STATUS register with a same definition in the task files, in which the Host writes the COMMAND/STATUS register to issue an AT attachment (ATA) command, and reads the COMMAND/STATUS register to obtain a programming status.

26. The method of claim 25, wherein the method comprises using two commands in the redefined task files to enter or leave the flash ROM programming mode and two commands to start reading or writing data on the flash ROM.

27. The method of claim 24, wherein the task files used by the IDE interface comprise an AT attachment (ATA) specification.

28. The method of claim 19, further comprises reinterpreting all bus activities so that the flash ROM is updated without using definitions of the interface.

29. A system for programming a flash read-only memory (ROM), the system communicating with a host computer (Host) through an interface comprising ATA task files, the system comprising:

the host for transmitting programming information to the flash ROM through the interface with the ATA task files during a programming mode;

a flash controller coupled to the Host through the interface, wherein the programming information from the Host directly programs the flash ROM

through the flash controller which interprets task files used by the Host to write data into the flash ROM or to read data from the flash ROM;

the flash ROM, coupled to the flash controller; and

a microprocessor coupled to the flash controller, the microprocessor being without access to the flash ROM while the flash ROM is in the programming mode.

30. The system of claim 29, wherein the interface is an IDE interface and the Host redefines registers of the task files so that definitions of the IDE interface is redefined according to the redefined registers of the task files during the programming mode.

31. The system of claim 30, wherein the Host switches the system into the programming mode through a flash_on command of the control commands under the re-defined IDE interface and the re-defined registers of the task files, and leaves the programming mode through a flash_off command of the control commands to return the original definitions of the IDE interface and the registers of the task files.

32. The system of claim 30, wherein the flash controller receives read/write activities to the redefined task files from the Host and reinterprets the read/write activities to perform writing or reading data on the flash ROM through a software cycle or a hardware cycle.

33. The system of claim 32, wherein the Host directly controls flash ROM pins to transfer the data through the flash controller in the software cycle.

34. The system of claim 32, wherein the re-defined registers of the task files in the software cycle comprise:

a CTL register defined as a control mapped to the flash ROM pins of cs#, wr#, and oe#, in which the Host can use the CTL register to control a status of the pins;

a DBUS register defined as a data bus mapped to the flash ROM pins of data bus, in which the Host can use the DBUS register to control a status of the pins;

an ABUSLOW register defined as an address bus low mapped to the flash ROM pins of an address bus low byte, in which the Host can use the ABUSLOW register to control a status of the pins; and

an ABUSHIGH register defined as an address bus high mapped to the flash ROM pins of an address bus high byte, in which the Host can use the ABUSHIGH register to control a status of the pins.

35. The system of claim 32, wherein the flash controller transfers the data either to the Host or the flash ROM, depending on a desired purpose of writing or reading, through a memory buffer in the hardware cycle.

36. The system of claim 35, wherein the memory buffer comprises a random access memory (RAM) coupled to the flash ROM.

37. The system of claim 35, wherein the registers of the task files are redefined in the hardware cycle comprise:

a DATA register used as a data port and has a same definition in the task files;

a LENGTH register used as a transfer length to specify a transferring byte count of the data in the hardware cycle; and

a COMMAND/STATUS register with a same definition in the task files, in which the Host writes the COMMAND/STATUS register to issue an AT attachment (ATA) command, and reads the COMMAND/STATUS register to obtain a programming status.

38. The system of claim 32, wherein the software cycle is used in combination with the hardware cycle in the programming mode.

39. The system of claim 30, wherein original definitions of the task files used by the IDE interface are according to AT attachment (ATA) specification.

40. The system of claim 30, wherein the redefined registers of the task files comprise:

a DATA register used as a data port and has a same definition in the task files;

a LENGTH register used as a transfer length to specify a transferring byte count of the data in the hardware cycle;

a CTL register defined as a control mapped to the flash ROM pins of cs#, wr#, and oe#, in which the Host can use the CTL register to control a status of the pins;

a DBUS register defined as a data bus mapped to the flash ROM pins of data bus, in which the Host can use the DBUS register to control a status of the pins;

an ABUSLOW register defined as an address bus low mapped to the flash ROM pins of an address bus low byte, in which the Host can use the ABUSLOW register to control a status of the pins;

an ABUSHIGH register defined as an address bus high mapped to the flash ROM pins of an address bus high byte, in which the Host can use the ABUSHIGH

register to control a status of the pins;

a DRIVE_SELECT register defined as a drive select, in which the Host writes the DRIVE_SELECT register to select an IDE periphery device, and DRIVE_SELECT register has a same definition in the task files; and

a COMMAND/STATUS register with a same definition in the task files, in which the Host writes the COMMAND/STATUS register to issue an AT attachment (ATA) command, and reads the COMMAND/STATUS register to obtain a programming status.